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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/633,375	08/07/2000	Daniel R. Loughmiller	303.145US3	5476

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EXAMINER

KURIAN, ROSHNI

ART UNIT	PAPER NUMBER
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2829

DATE MAILED: 03/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/633,375

Applicant(s)

LOUGHMILLER ET AL.

Examiner

Roshni Kurian

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 August 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 19-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 August 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other: _____

Drawings

1. The drawings are objected to because the items 16 and 20 are not labeled in Figure 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the capacitor mentioned in Claims 26 and 33 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent-text-for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections

35 USC § 102 Rejections

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 19-22, 25-30 and 33-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al (US 6060896).

• Regarding Claim 19, Ma et al, in Figure 1, discloses a method for measuring a voltage at an internal node of an integrated circuit, the method comprising:

- coupling a pass circuit (8) between the internal node (10) and a pin of the integrated circuit;
- using a reset circuit (6) to activate the pass circuit (8); and
- driving the pass circuit (6) to pass the voltage from the internal node to the pin.

Regarding claim 20, Ma et al, in Figure 1, discloses a method, further comprising using a pass control (4) circuit to drive the pass circuit (8).

- Regarding claim 21, Ma et al, in Figure 1, discloses a method, further comprising using the pass control (4) circuit to provide at least one output signal (18) to selectively drive the pass circuit (8) to pass a voltage from the internal node to the pin, thereby allowing the voltage at the internal node to be read after the integrated circuit is packaged.

- Regarding Claim 22, Ma et al, in Figure 1, discloses a method, wherein the pass control (4) circuit comprises an n-channel MOS transistor (42) having a drain coupled to the internal node, the n-channel MOS transistor configured to, when turned on, pass the voltage at the internal node to a source of the n-channel MOS transistor and to the pass circuit (8).

- Regarding Claim 25, Ma et al, in Figure 1, discloses a method, further comprising using a pass control circuit to apply a desired voltage to the internal node, thereby forcing the voltage at the internal node to the desired voltage.

- Regarding Claim 26, Ma et al, in Figure 1, discloses a method, wherein the pass circuit comprises: a pass gate (54) having first, second, and third terminals, the first terminal (18) coupled to a pass control circuit (4), the second terminal (20) coupled to the internal node, the third terminal (16) coupled to the pin; and a capacitor coupled between the first terminal of the pass gate and the pass control circuit such that a voltage at the first terminal of the pass gate is driven to cause a voltage at the second

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terminal voltage to be passed to the third terminal for reading the voltage at the internal node.

- Regarding Claim 27, Ma et al, in Figure 1, discloses a method wherein the pass gate comprises an n-channel MOS transistor (50).

- Regarding Claim 28, Ma et al, in Figure 1, discloses a method for forcing a voltage at an internal node of an integrated circuit to a desired level, the method comprising:

- coupling a pass circuit (4) between the internal node (10) and a pin of the integrated circuit; applying a voltage of the desired level to the pin;
- using a reset circuit (6) to activate the pass circuit (4); and
- driving the pass circuit (4) to pass the applied voltage from the pin to the internal node, thereby forcing the voltage at the internal node to the desired level.

- Regarding Claim 29, Ma et al, in Figure 1, discloses a method, further comprising using a pass control (4) circuit to drive the pass (8) circuit.

- Regarding Claim 30, Ma et al, in Figure 1, discloses a method wherein the pass control (4) circuit comprises an n-channel MOS transistor (42) having a drain coupled to the internal node, the n-channel MOS transistor configured to, when turned on, pass the voltage at the internal node to a source of the n-channel MOS transistor and to the pass circuit (8).

- Regarding Claim 33, Ma et al, in Figure 1, discloses a method wherein the pass circuit comprises: a pass gate (54) having first, second, and third terminals, the

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first terminal (18) coupled to a pass control circuit (4), the second terminal (20) coupled to the internal node, the third terminal (16) coupled to the pin; and a capacitor coupled between the first terminal of the pass gate and the pass control circuit such that a voltage at the first terminal of the pass gate is driven to cause a voltage at the second terminal voltage to be passed to the third terminal for reading the voltage at the internal node.

- Regarding Claim 34, Ma et al, in Figure 1, discloses a method wherein the pass gate comprises an n-channel MOS transistor (50).

35 USC § 103 Rejections

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 23-24 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al (US 6060896), and in view of Mitsui (US 5999009).

- Regarding Claim 23 and 24, Ma et al does not disclose that a ring oscillator is use to provide an oscillating control signal to the pass circuit. However, Mitsui, in Figure 1, discloses a method wherein a ring oscillator (21) is utilized to provide an oscillating control signal to the pass circuit (23). It would have been obvious to one of ordinary skill in the art to modify the apparatus taught by Ma et al in view of Mitsui to incorporate the ring oscillator so as to achieve a precise control means.

Regarding Claim 31 and 32, Ma et al does not disclose that a ring oscillator is use to provide an oscillating control signal to the pass circuit. However, Mitsui, in Figure 1, discloses a method wherein a ring oscillator (21) is utilized to provide an oscillating control signal to the pass circuit (23). It would have been obvious to one of ordinary skill in the art to modify the apparatus taught by Ma et al in view of Mitsui to incorporate the ring oscillator so as to achieve a precise control means.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roshni Kurian whose telephone number is (703) 308-7607. The examiner can normally be reached on Monday - Friday, 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (703) 308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7607 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-4900.

RK
March 6, 2002



3-11-02

MICHAEL J. SHERRY
PRIMARY EXAMINER